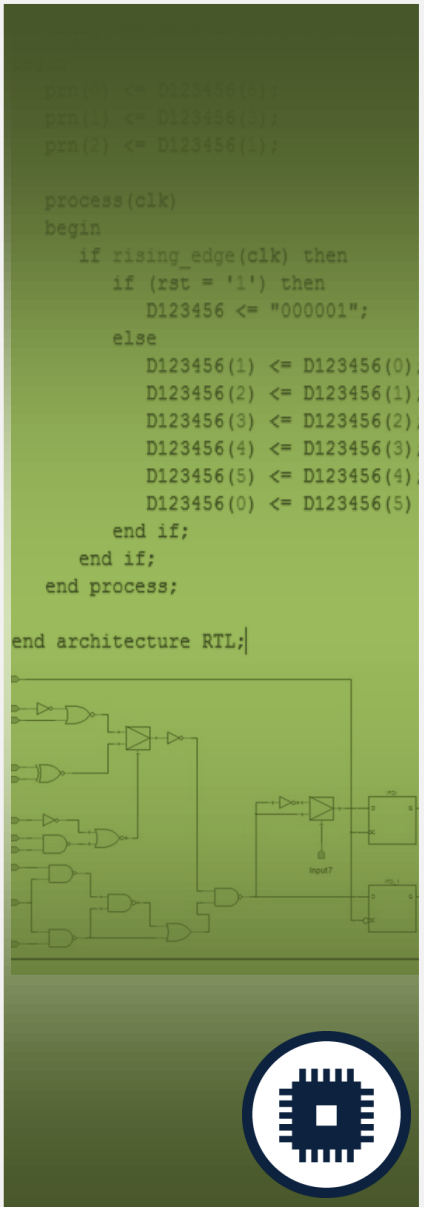
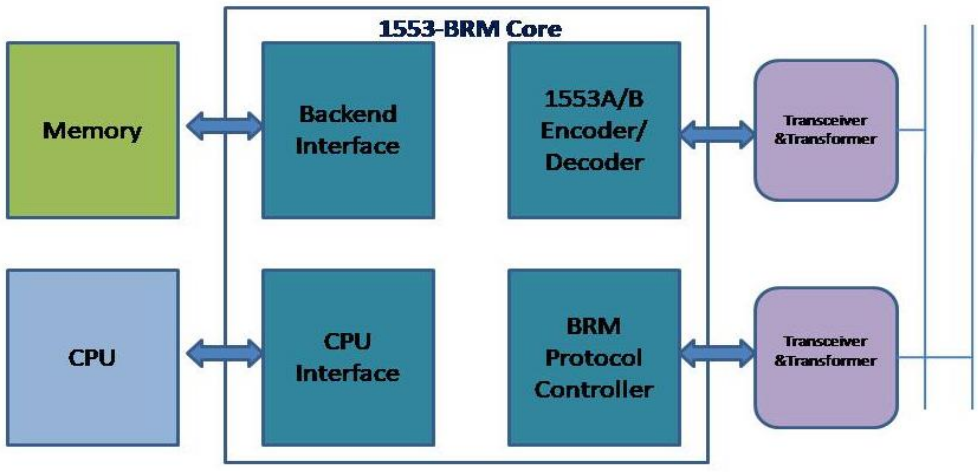
Mil-Std-1553 BRM Cores for FPGAs/ASICs

Key Features

- Mil-Std-1553 Intellectual Property for FPGAs and ASIC .
- VHDL and Verilog RTL code - Vendor and technology independent
- Also Available in Netlist form for different families of leading FPGA Vendors
- Suitable for any MIL-STD-1553 Bus Controller (BC), Remote Terminal (RT) and Bus Monitor (BM) implementation
- Common Core, which can be configured in RT,BC and BM
- Also available in Individual or Dual Functions mode
- Compatible to Enhanced DDC® Mini-Ace®and Micro-Ace® interface and functionality, works with existing software drivers
- Optimized code -Small FPGA area /Gate Counts
- Modular architecture allowing flexible implementations
- Provided with full verification environment - UVM based automated bench
- RT Validation Test Plan MIL-HDBK-1553, Appendix A complied





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IP CORE - MIL-STD-1553

Specifications

Remote Terminal
- Notice 2 Notice II Compliant
- 16-Bit Time Tag

RT Advanced Features
- Circular Buffer
- Command legalization
- Indexing
- RT Validated according to test plan from MIL-HDBK-1553A

1Mbps Data Rate

Selectable Clock Rate
- 12, 16, 20 or 24 MHz

Connects to any transceiver transformer

Bus Controller
- Timeout retries
- Status Polling
- Conditional Branching and Sub-Routines

Monitor Terminal
- Can operate simultaneously with RT

CPU Interface
- Provides Direct CPU Access to Memory

Memory
- 1 Kb to 128 Kb (16-bits wide)

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Description

The IP-Core 1553 BRM provides a complete, MIL-STD-1553 Bus Controller (BC), Remote Terminal (RT), or Monitor Terminal (MT).The IP-Core 1553 BRM requires connection to an external CPU this is used to set up the core and initialize the data tables in memory. The external memory block is used to store the received and transmitted data. This memory can be internal or external to the FPGA/ASIC. The core interfaces to the 1553 bus through an external 1553 transceiver and transformer.

Verification and Compliance

The IP-Core 1553 BRM is fully verified against the RT Validation Test Plan (MIL-HDBK-1553A, Appendix A). This ensures that the 1553B encoders and decoders are fully compliant with the 1553B specification. The validation of the IP-Core 1553 BRM has been carried out with industry standards 1553 devices.

Programmability

The IP-Core 1553 BRM can be configured for 1553A or 1553B modes , different clock frequencies and for other optional features. Same core can be used in dual modes RT as well as in BM mode simultaneously.

Synthesis and Simulation Support

Supported to FPGA IDEs like ISE, Vivado, Libero ,Quartous
Synthesis: Exemplar, Synplicity®, Design Compiler®,FPGA Compiler™, Simplify premier
Simulation: Questasim, VCS

Supported FPGA Families

The IP-Core 1553 BRM has been successfully implemented in the leading FPGAs like Xilinx -V-4/5/6/7 Zynq , Microsemi -RTAX2000, 54SX72A, and Altera. The IP-Core 1553 BRM can be used in ASICs development as it is technology and vendor independent.

Deliverables

The IP-Core 1553 BRM is delivered in form of
Netlist Version –– Compiled RTL Simulation Model, Compliant with the Integrated Design Environment (IDE) for the selected FPGA
or
RTL Version – VHDL and Verilog Core Source Code ,Synthesis Scripts and UVM Testbench along with user's manual.