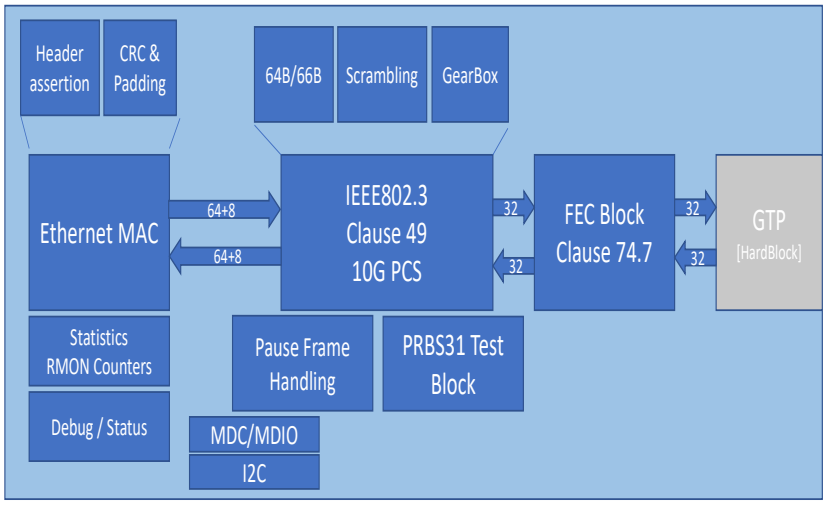
IP Core – Ethernet

10 Gb/s ,25Gb/s, 40Gb/s Ethernet MAC Logic Core

Key Features

- Full-duplex MAC, fully compliant to IEEE802.3
- 64 bit wide data bus for 10G and 128 bit wide bus for 40G and 25G.
- Implements MAC functions like – Padding, FCS insertion and verification, Receive error handling and MIB counters
- Options for MAC headers insertion[MAC_DA + MAC_SA + Type or MAC_DA + MAC_SA + Type + VLAN]
- Programmable promiscuous (transparent) mode.
- Max delay through MAC layer is 6 clocks per direction [4 for FCS, 2 for FIFO read delays]
- Unidirectional [optional] feature specified by IEEE 802.3 (Clause 66). Priority-based flow control (PFC) with programmable pause quanta, supporting two to eight priority queues.



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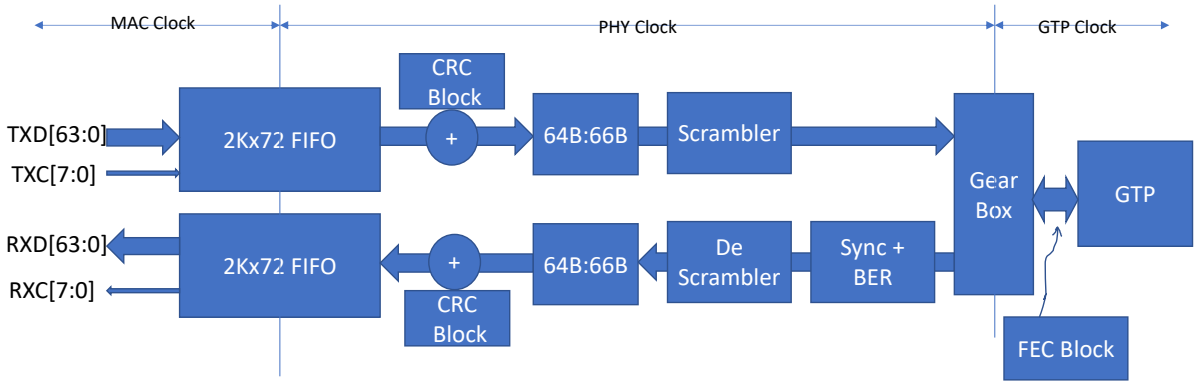
Standard Compliance:

- Reconciliation Sublayer as per section 46 [10G], 81[40G]
- PCS layer as design as per section 49 [10G] , 82[40G]
- Physical Media Dependent Layer [Section 72 and 71] for 10G Base KR and 10G Base-KX4 [using GTPs for FPGA]
- Autonegotiation over backplanes [Section 73]
- Forward Error Correction for Base-R Phys [section 74]
  - Cyclic FEC for KR specification as per section 74
  - RS encoding extension as an option for 25G Ethernet

Interfaces:

- Client side 128 bit wide bus for 40G and 64 bit wide bus [can be modified to 32 bit] for 10G.
- Line side interface – 10G Base KR or 10G Base R with GTP supported by FPGAs.



Frame Structure Control Features:

- Virtual local area network (VLAN) and stacked VLAN tagged frames decoding (Configurable Type . Normally 0x8100)
- 2112-2080 Shortened Cyclic redundancy code [section 74.7.4.4] computation and insertion on the TX datapath
- Deficit idle counter (DIC) for optimized performance with average inter-packet gap (IPG) for LAN applications. Supports programmable IP.
- Ethernet flow control using pause frames.
- Programmable maximum length of transmit (TX) and receive (RX) data frames up to 64 kilobytes (KB).
- Programmable Preamble for special custom purposes
- Optional padding insertion on the TX datapath and termination on the RX datapath.
- PRBS31 based link error check and BER report [Programmable for the run for certain time period or free run.